Amendments to the Drawings

The attached sheet of drawings includes a change to Fig. 3. This sheet replaces the original sheet including Fig. 3. In Fig. 2, the connection of output transistor 2322 is changed from drive pulse V1 to drive pulseV2.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS

I. Introduction

Claims 1-14 are pending in this application, of which claims 1 and 10 are independent. In this Amendment, claims 1 and 10 have been amended. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the amendment of claim 1 can be found on, for example, page 23, lines 9-14 of the specification. Adequate descriptive support for the amendment of claim 10 can be found on, for example, page 27, lines 20-26 of the specification. The specification has also been amended to correct minor errors. In addition, Fig. 3 has been amended based on page 19, lines 12-14 of the specification.

II. The Present Invention

Before discussion of the rejection of claims 1-14, a brief explanation of the present invention is provided.

A conventional MOS type imaging apparatus manufactured based on a CMOS processing technology might suffer, in the imaging region, leakage current in a photodiode unit and deterioration of properties in an amplification circuit during a driving operation, which causes noise. When noise is caused in the imaging region, it is amplified and output with the signal charge, resulting in deterioration of image quality.

In view of the above problem, the present invention aims to provide a solid-state imaging apparatus that realizes less leakage current, high image quality and low noise during the driving operation, and manufacturing method for the same.

The solid-state imaging apparatus according to amended claim 1 requires all the transistors in the imaging region and the drive circuit region have the same channel polarity. The

manufacturing method for a solid-state imaging apparatus according to amended claim 10 requires that all transistor formed in both steps for forming the imaging region and the drive circuit region, respectively are MOS type transistors having the same channel polarity.

According to the claimed apparatus, since all the transistors in the imaging region and the drive circuit region have the same channel polarity, the number of processes required for forming the transistors in both regions is approximately half the number of processes required for forming the transistors of the conventional solid-state imaging apparatus with use of the conventional CMOS processing technology. This means that the imaging region of the claimed invention suffers less damage during the process of forming the transistors.

III. The Rejection of Claims 1-5, 10 and 11

Claims 1-5, 10 and 11 have been rejected under 35 U.S.C. §102(b) as being anticipated by Yuzurihara et al. Yuzurihara et al. discloses a solid-state imaging apparatus with n-type MOS transistors formed in an imaging region and n-type MOS transistors and p-type MOS transistors formed in a peripheral circuit by a CMOS process.

Applicant submits that Yuzurihara et al. does not disclose a solid-state imaging apparatus including all the limitations recited in independent claim 1. Specifically, Yuzurihara et al. does not disclose, among other things, that "all the transistors in the imaging region and the drive circuit region have a same channel polarity," as recited by independent amended claim 1.

In contrast, Yuzurihara's transistors in the driving circuit region are formed by a CMOS process, and p-type MOS transistors are formed as well. Accordingly, in the solid-state imaging apparatus disclosed by Yuzurihara et al., the conductivity type of some transistors in the driving circuit region is different from the conductivity type of the transistors in the imaging region.

This configuration is similar to the conventional configuration of the solid-state imaging apparatus based on the CMOS process.

Accordingly, Applicant submits that Yuzurihara et al. does not disclose a solid-state imaging apparatus including all the limitations recited in independent claim 1, as amended. The above discussion is also applicable to independent claim 10, and thus, claim 10 is patentable over Yuzurihara et al. Dependent claims 2-5 and 11 are also patentably distinguishable over Yuzurihara et al. at least because those claims respectively include all the limitations recited in independent claims 1 and 10. Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1-5, 10 and 11 under 35 U.S.C. §102(b) and favorable consideration thereof.

III. The Rejection of Claims 6-8 and 12-14

Claims 6-8 and 12-14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yuzurihara et al. in view of Momose et al. In response, Applicant submits that dependent claims 6-8 and 12-14 are patentably distinguishable over Yuzurihara et al. and Momose et al. at least because those claims respectively include all the limitations recited in independent claims 1 and 10.

Applicant specifically notes that Momose et al. does not cure the deficiencies of Yuzurihara et al. Momose et al. discloses a MOS transistor in which the gate length is equal to or less than 0.6 μm and the thickness of the gate insulating film is less than 2.5 μm, but does not disclose, among other things, that "all the transistors in the imaging region and the drive circuit region have a same channel polarity," recited in independent claim 1, as amended.

Momose et al. does not disclose that all the transistors formed in the imaging region and the driving circuit region are of the same conductivity type (only n-type transistors or only p-type

transistors). The reference only discloses the structure of a MOS transistor in a common logical device.

Accordingly, it is submitted that the applied combination of Yuzurihara et al. and Momose et al. does not disclose or teach a solid-state imaging apparatus and a manufacturing method including all the limitations recited in claims 6-8 and 12-14. Applicant, therefore, respectfully solicit withdrawal of the rejection of claims 6-8 and 12-14 under 35 U.S.C. §103(a) and favorable consideration thereof.

IV. The Rejection of Claim 9

Claim 9 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yuzurihara et al. in view of Shinohara et al. In response, Applicant submits that dependent claim 9 is patentably distinguishable over Yuzurihara et al. and Shinohara et al. at least because it includes all the limitations recited in independent claim 1. Applicant specifically notes that Shinohara et al. does not cure the deficiencies of Yuzurihara et al.

Applicant, therefore, respectfully solicits withdrawal of the rejection of claim 9 under 35 U.S.C. §103(a) and favorable consideration thereof.

V. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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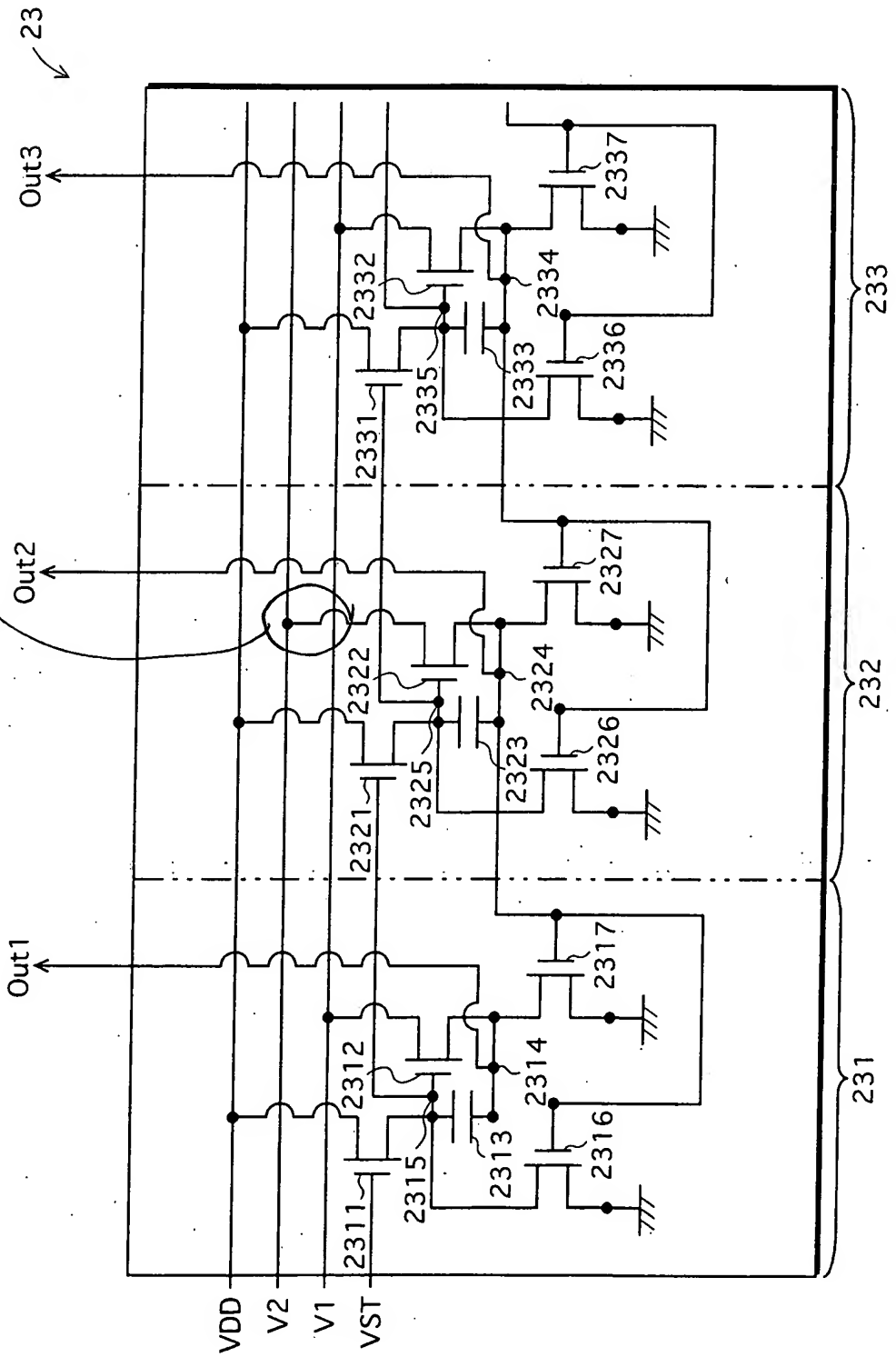
FIG.3



Connected to V2